Computer Architecture Lec 5b

Dr. Esti Stein

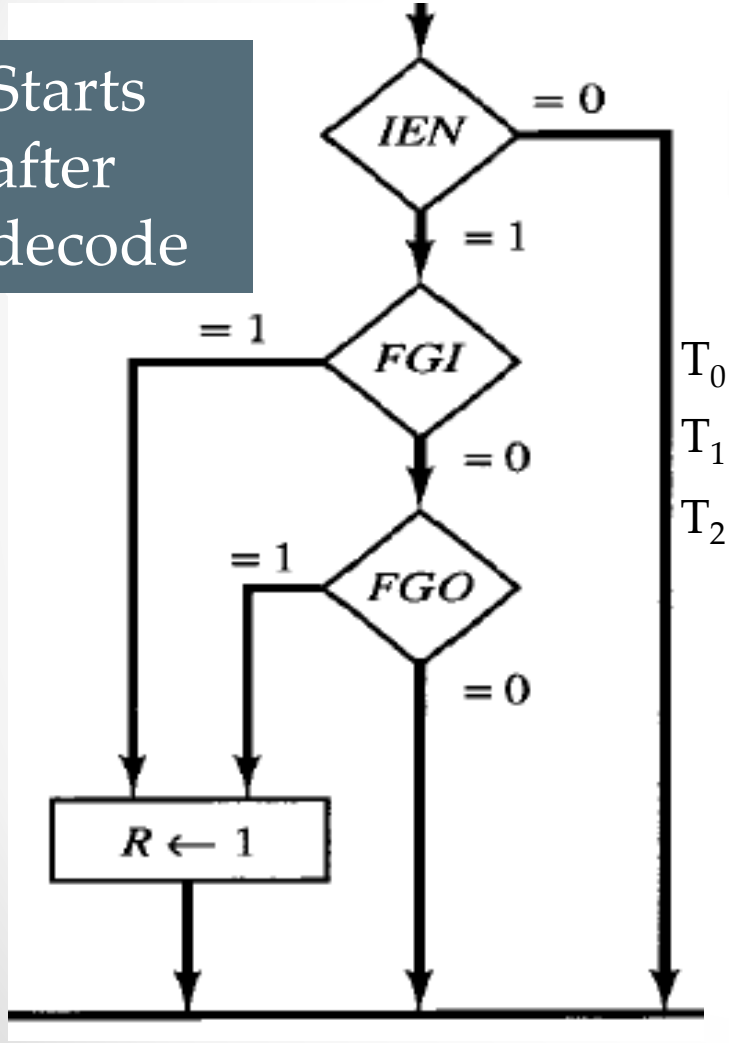
(Partly taken from Dr. Alon Schclar slides)

Based on slides by:
Prof. Myung-Eui Lee
Korea University of Technology & Education
Department of Information & Communication

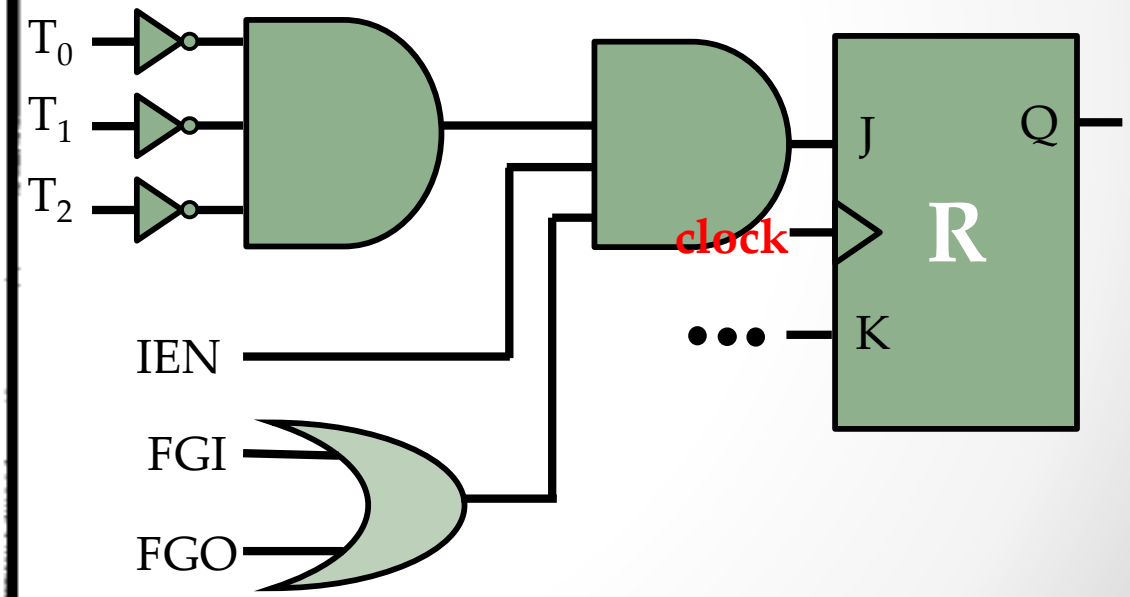
Taken from: **M. Mano/Computer Design and Architecture 3rd Ed.**

Going to Interrupt Cycle

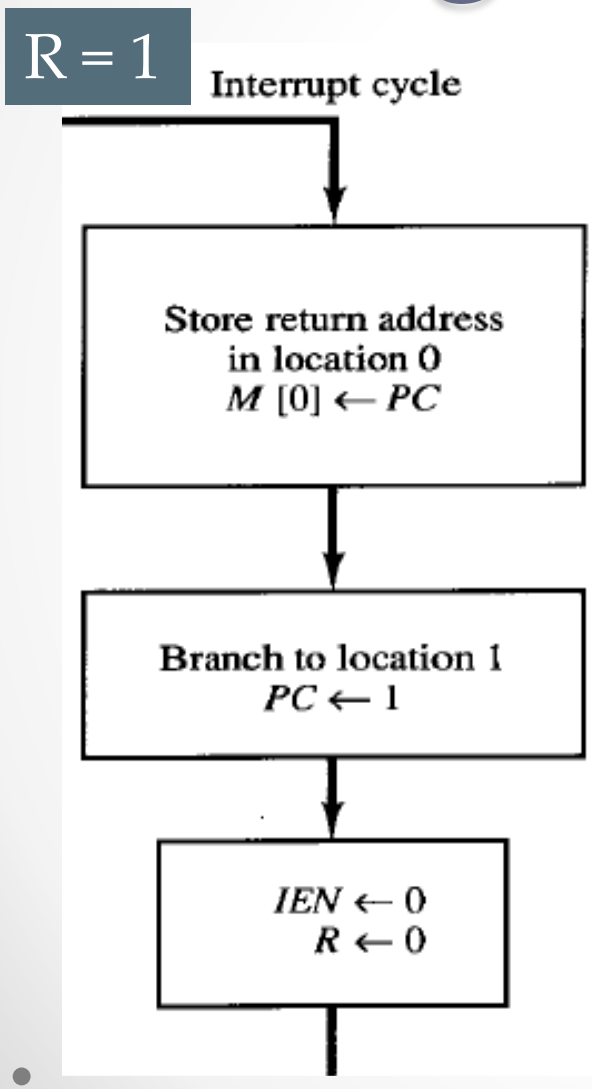
Starts after decode

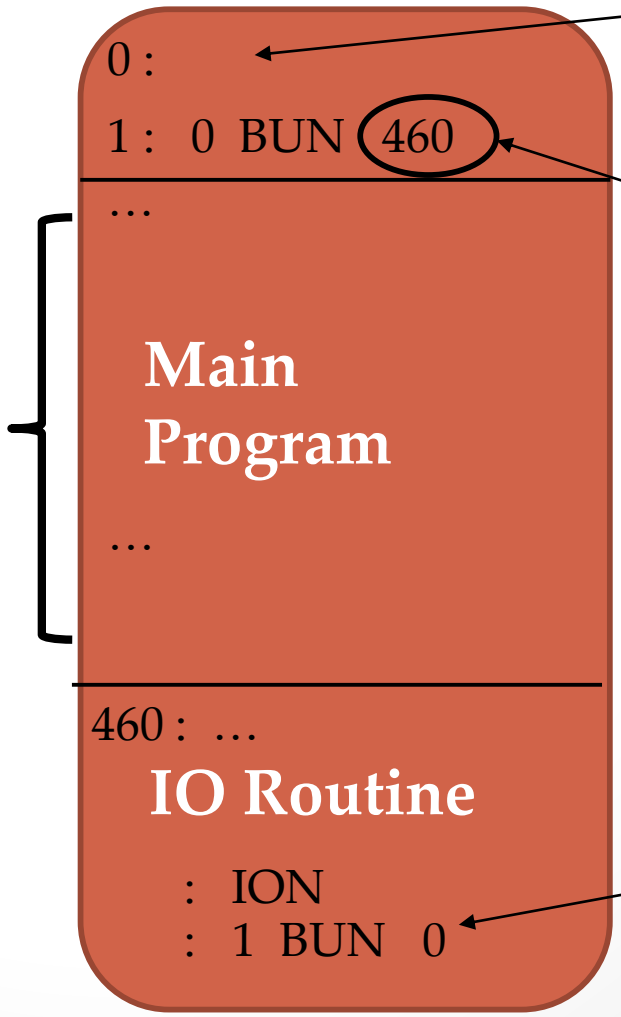


$T_0'T_1'T_2'(IEN)(FGI+FGO) : R \leftarrow 1$



Interrupt Routine Arrangement in Memory





Don't care

Always the address of the IO service routine

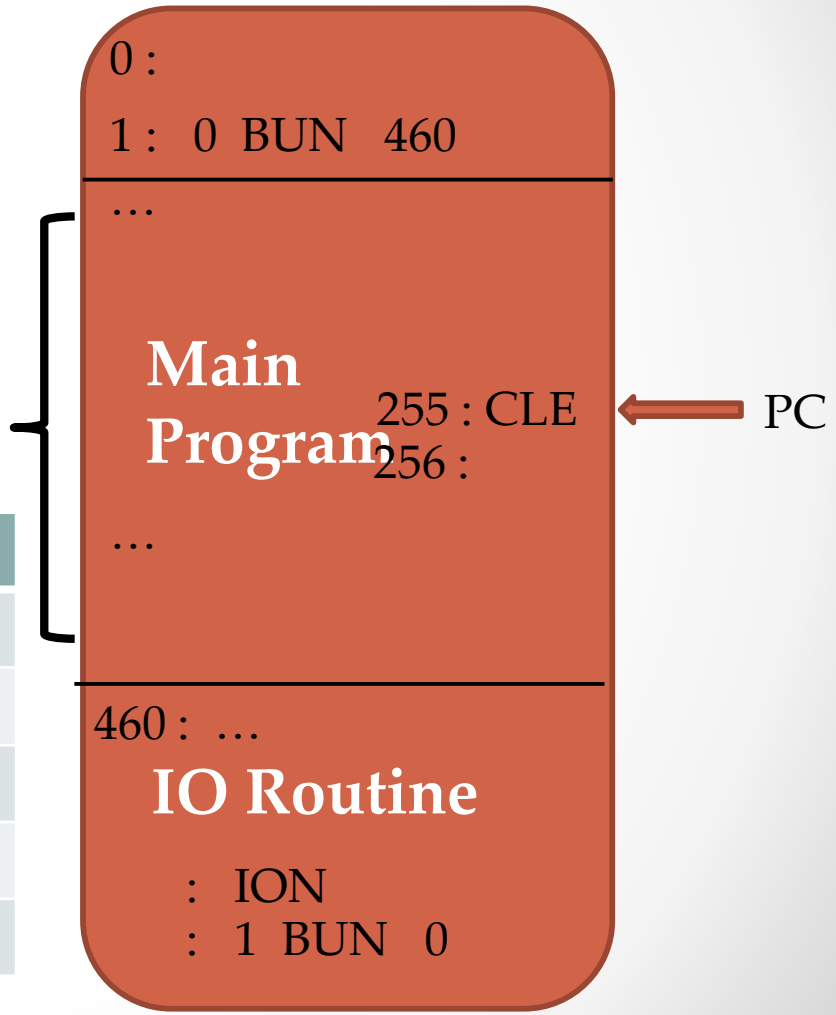
Always the last instruction in the routine

QUIZ2

Consider:
PC = 255 , T_0 = 1, IEN = 1,
FGI = 1, E = 1

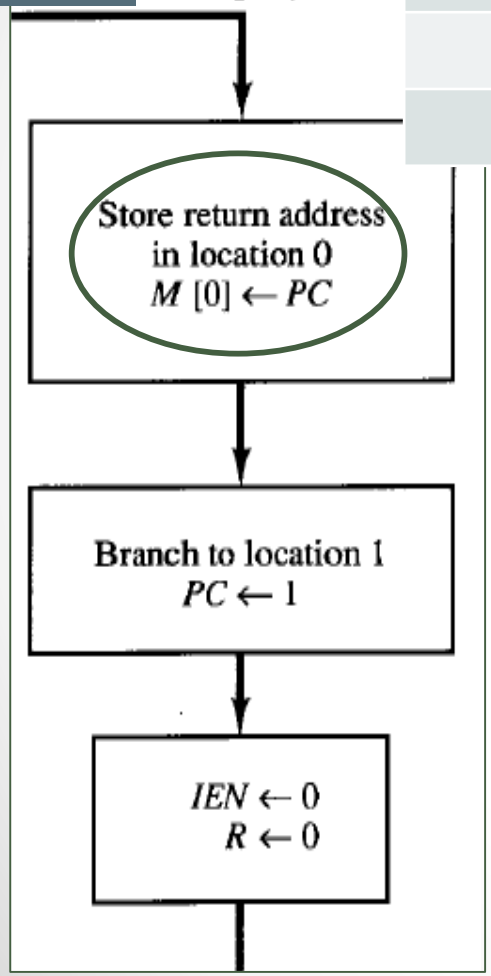
Determine the content of the registers below after each tick of the sequence counter

I	E	PC	AR	IR	R	Tick end
-	1	255	-	-	0	initial
						T_0
						T_1
						T_2
						T_3



Interrupt Cycle Execution

R = 1



IEN	TR	PC	AR	R	tick
1		256		1	T_0
					T_1
					T_2

$R'T_0$: AR ← PC

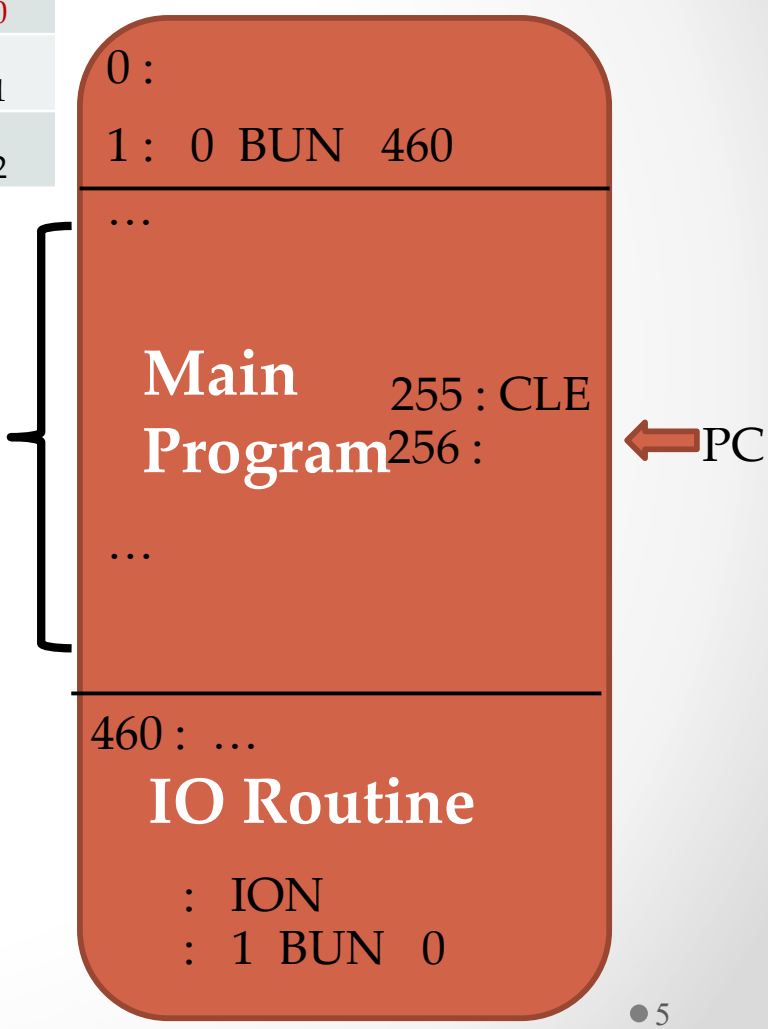
RT_0 : AR ← 0, TR ← PC

$R'T_1$: IR ← M[AR],
PC ← PC + 1

RT_1 : M[AR] ← TR ,
PC ← 0

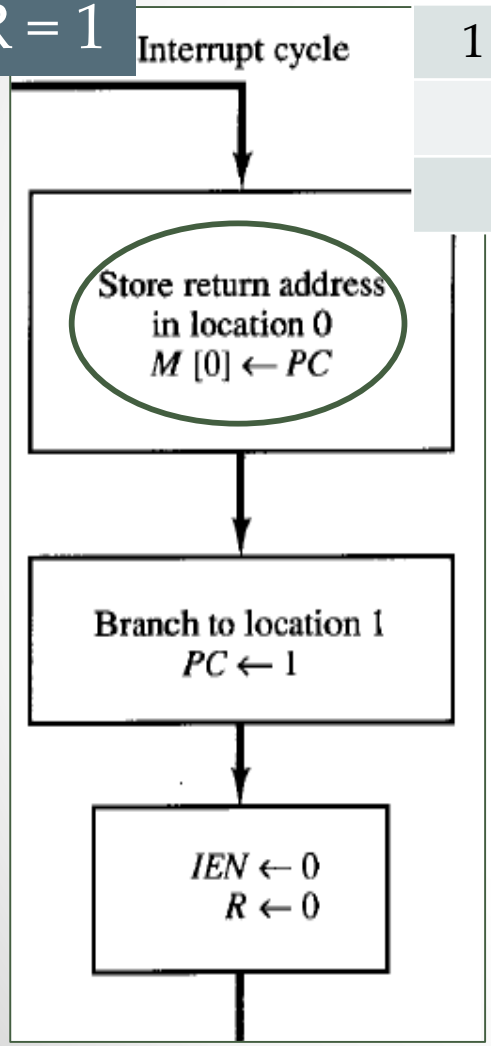
$R'T_2$: D_0 ,.., D_7 ←
Decode IR(12-14)
AR ← IR(0-11),
I ← IR(15)

RT_2 : PC ← PC + 1,
IEN ← 0,
R ← 0, SC ← 0



Interrupt Cycle Execution

R = 1



IEN	TR	PC	AR	R	tick
1	256	256	0	1	T_0
					T_1
					T_2

$R'T_0$: AR ← PC

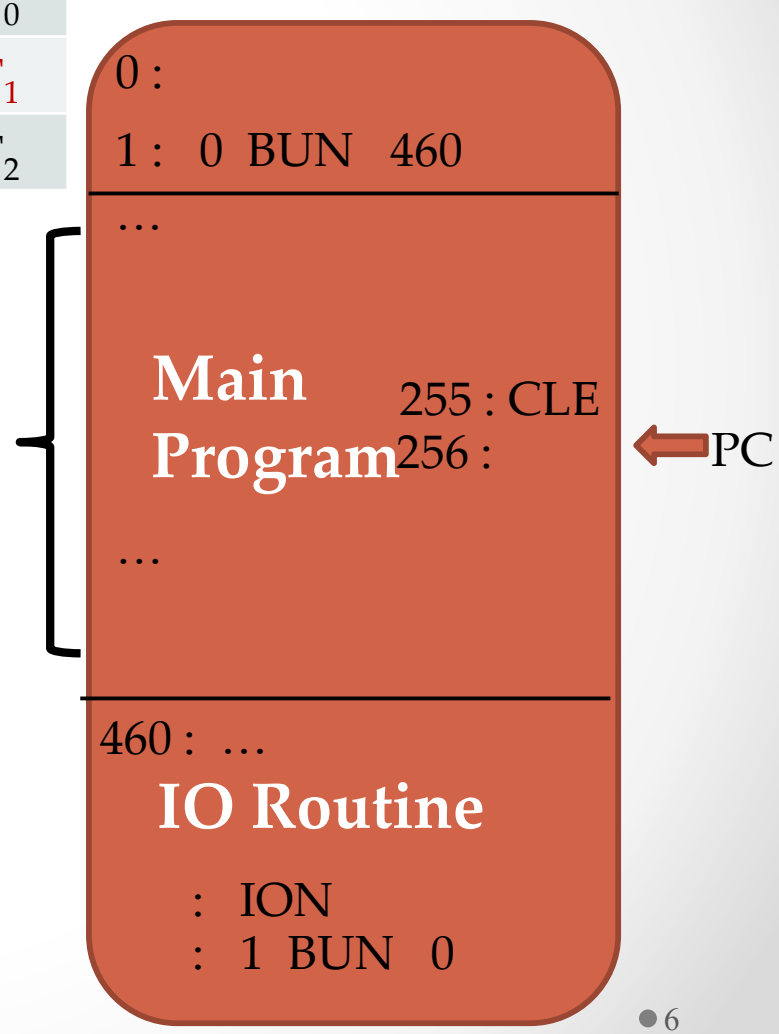
RT_0 : AR ← 0, TR ← PC

$R'T_1$: IR ← M[AR],
PC ← PC + 1

RT_1 : M[AR] ← TR ,
PC ← 0

$R'T_2$: D_0 ,.., D_7 ←
Decode IR(12-14)
AR ← IR(0-11),
I ← IR(15)

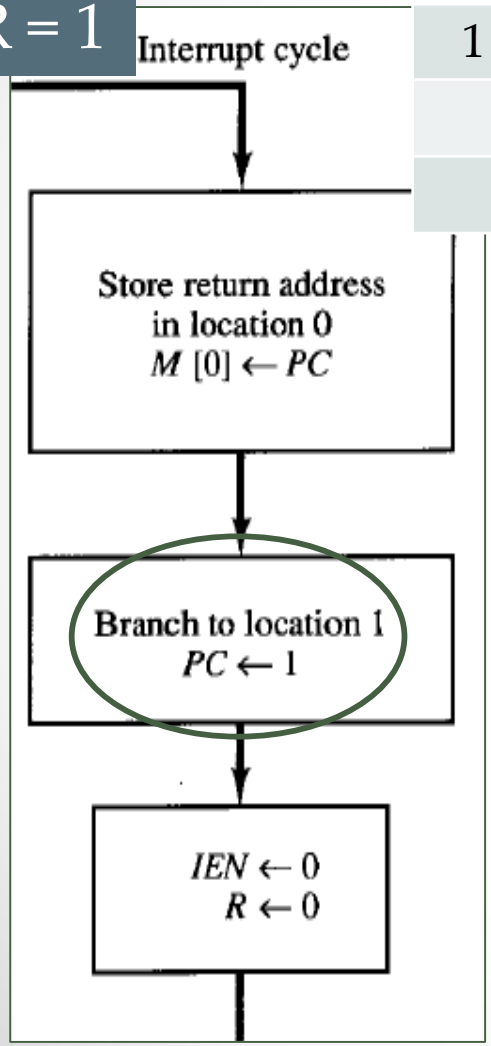
RT_2 : PC ← PC + 1,
IEN ← 0,
R ← 0, SC ← 0



Interrupt Cycle Execution

IEN	TR	PC	AR	R	tick
1	256	256	0	1	T_0
					T_1
					T_2

R = 1



$R'T_0$: AR ← PC

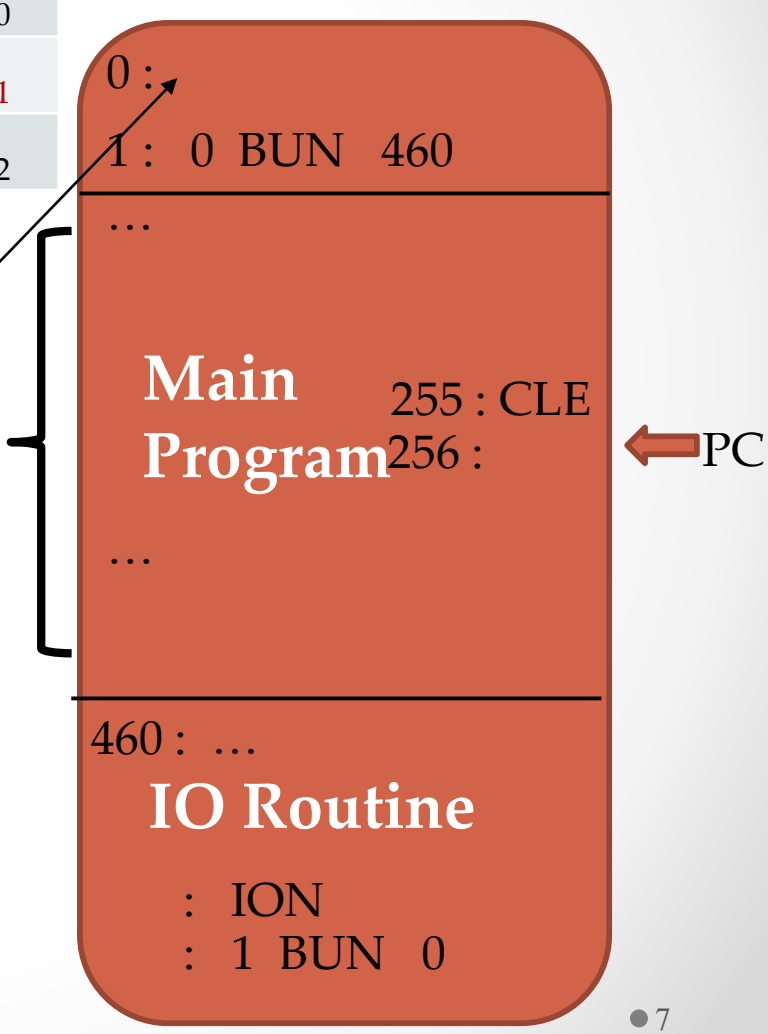
RT_0 : AR ← 0, TR ← PC

$R'T_1$: IR ← M[AR],
PC ← PC + 1

RT_1 : M[AR] ← TR ,
PC ← 0

$R'T_2$: D_0 ,.., D_7 ←
Decode IR(12-14)
AR ← IR(0-11),
I ← IR(15)

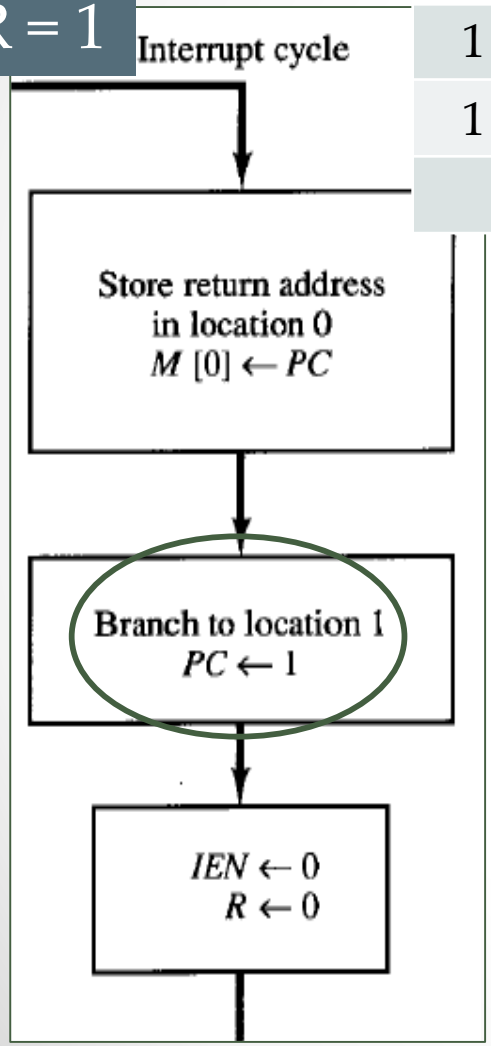
RT_2 : PC ← PC + 1,
IEN ← 0,
R ← 0, SC ← 0



Interrupt Cycle Execution

IEN	TR	PC	AR	R	tick
1	256	256	0	1	T_0
1	256	0	0	1	T_1
					T_2

R = 1



$R'T_0$: AR ← PC

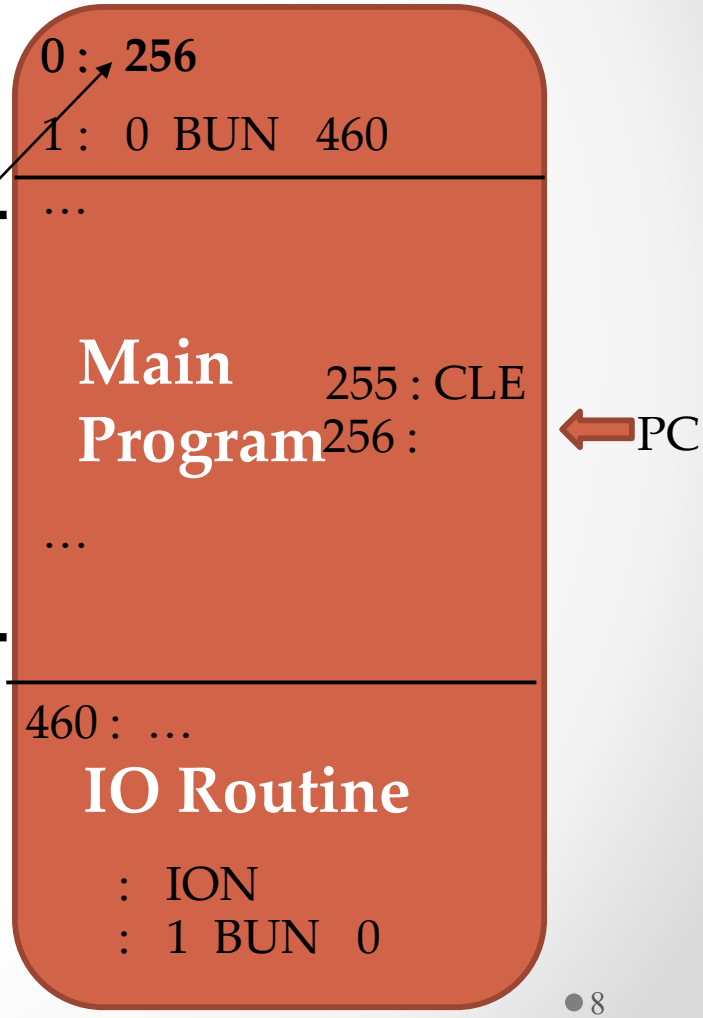
RT_0 : AR ← 0, TR ← PC

$R'T_1$: IR ← M[AR],
PC ← PC + 1

RT_1 : M[AR] ← TR ,
PC ← 0

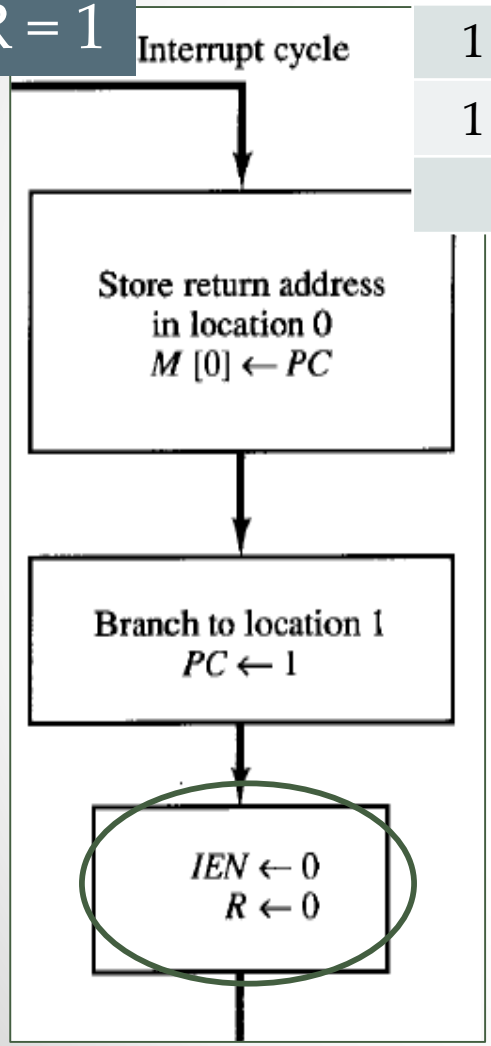
$R'T_2$: D_0 ,.., D_7 ←
Decode IR(12-14)
AR ← IR(0-11),
I ← IR(15)

RT_2 : PC ← PC + 1,
IEN ← 0,
R ← 0, SC ← 0



Interrupt Cycle Execution

R = 1



IEN	TR	PC	AR	R	tick
1	256	256	0	1	T_0
1	256	0	0	1	T_1
					T_2

$R'T_0$: AR ← PC

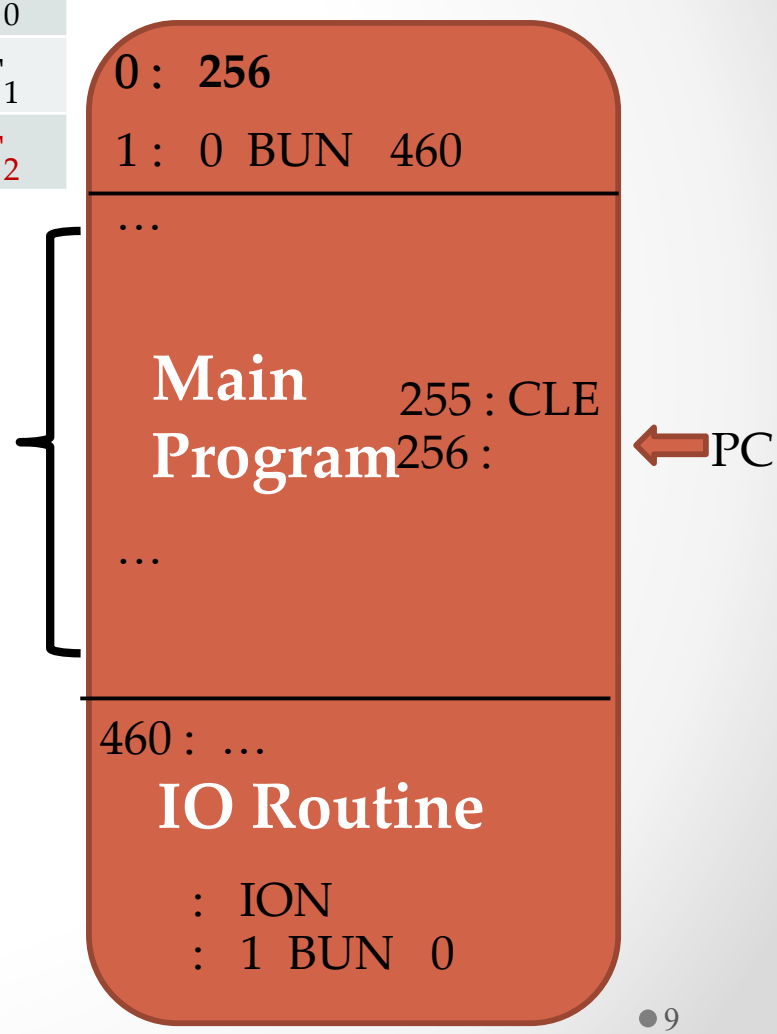
RT_0 : AR ← 0, TR ← PC

$R'T_1$: IR ← M[AR],
PC ← PC + 1

RT_1 : M[AR] ← TR ,
PC ← 0

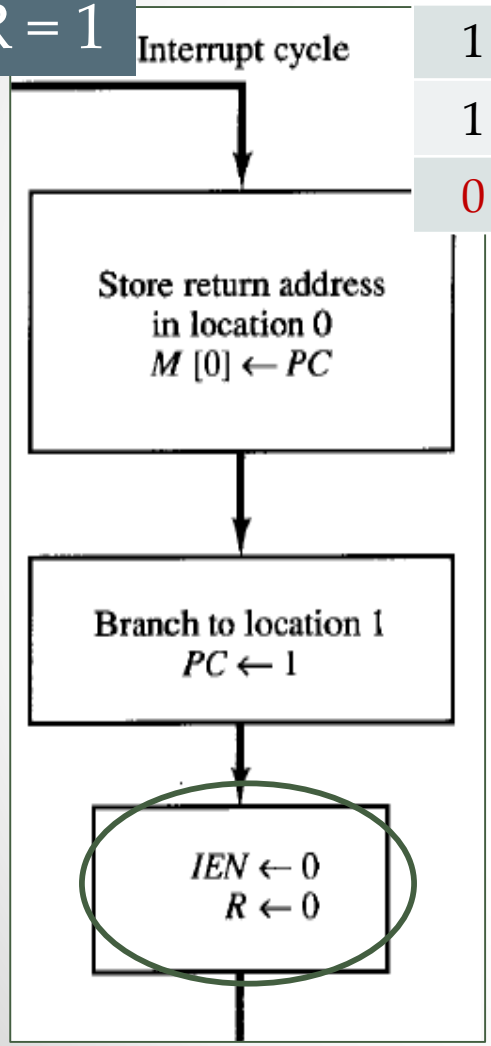
$R'T_2$: D_0 ,.., D_7 ←
Decode IR(12-14)
AR ← IR(0-11),
I ← IR(15)

RT_2 : PC ← PC + 1,
IEN ← 0,
R ← 0, SC ← 0



Interrupt Cycle Execution

R = 1



IEN	TR	PC	AR	R	tick
1	256	256	0	1	T_0
1	256	0	0	1	T_1
0	256	1	0	0	T_2

$R'T_0$: AR ← PC

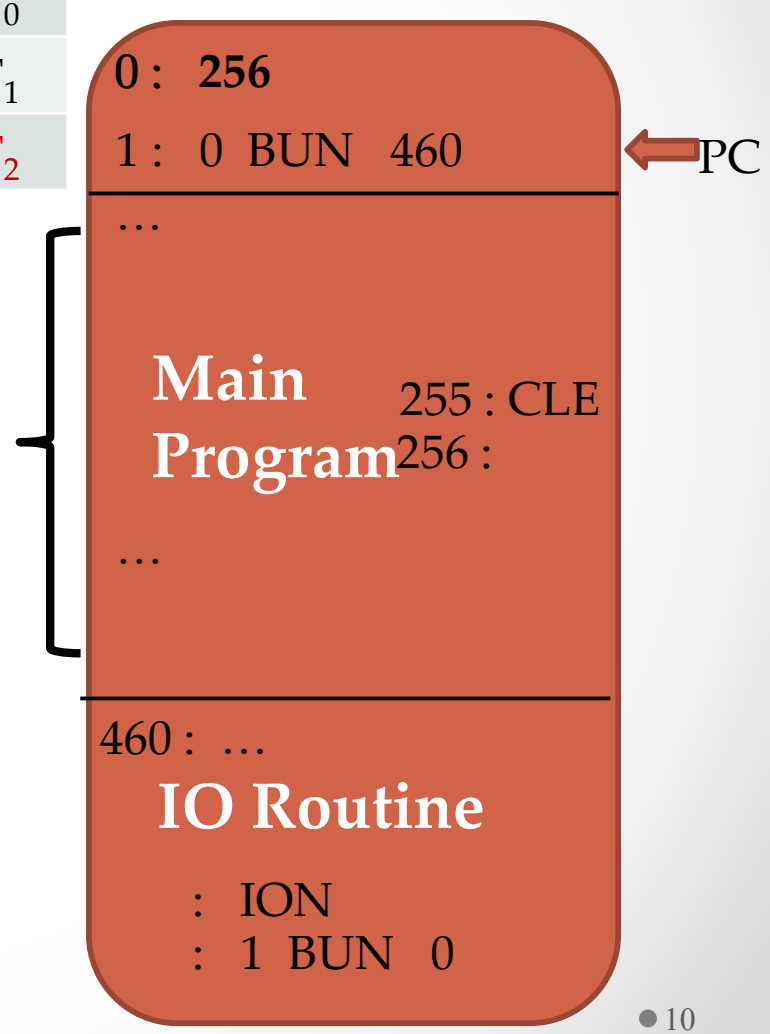
RT_0 : AR ← 0, TR ← PC

$R'T_1$: IR ← M[AR],
PC ← PC + 1

RT_1 : M[AR] ← TR ,
PC ← 0

$R'T_2$: D_0 ,.., D_7 ←
Decode IR(12-14)
AR ← IR(0-11),
I ← IR(15)

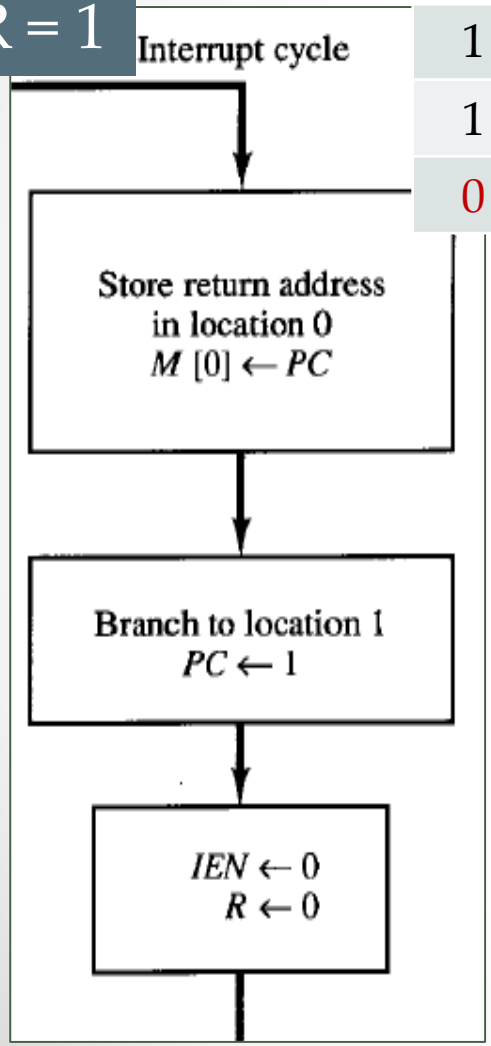
RT_2 : PC ← PC + 1,
IEN ← 0,
R ← 0, SC ← 0



Interrupt Cycle Execution

IEN	TR	PC	AR	R	tick
1	256	256	0	1	T_0
1	256	0	0	1	T_1
0	256	1	0	0	T_2

R = 1



$R'T_0$: AR ← PC

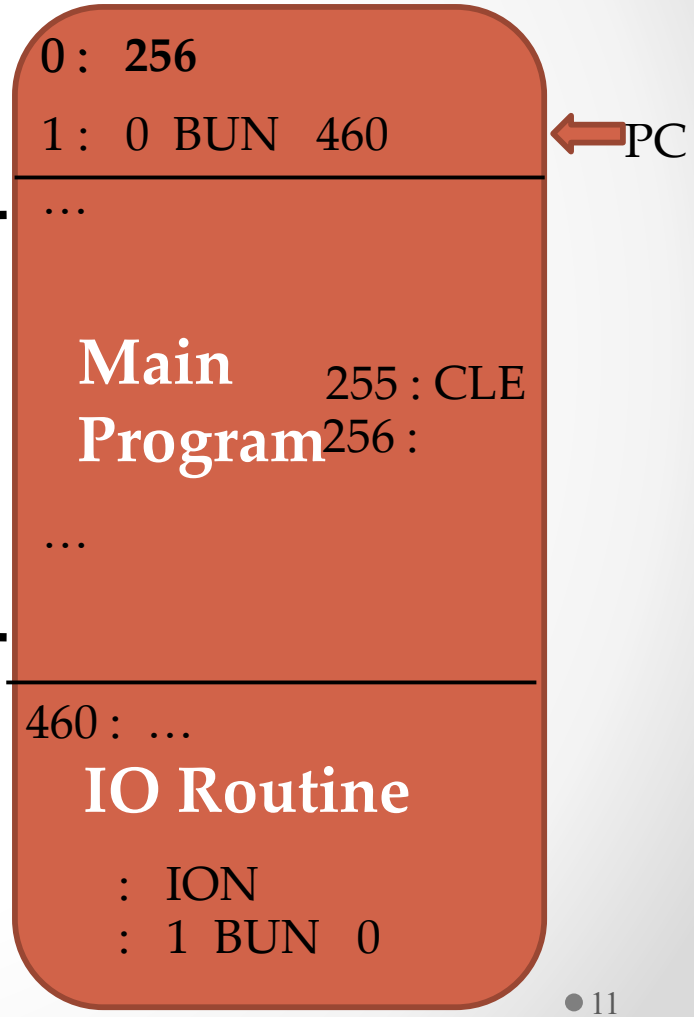
RT_0 : AR ← 0, TR ← PC

$R'T_1$: IR ← M[AR],
PC ← PC + 1

RT_1 : M[AR] ← TR ,
PC ← 0

$R'T_2$: D_0 ,.., D_7 ←
Decode IR(12-14)
AR ← IR(0-11),
I ← IR(15)

RT_2 : PC ← PC + 1,
IEN ← 0,
R ← 0, SC ← 0



QUIZ3

Determine the content of the registers at the end of the execution of each of the instructions mentioned below.

$R'T_0$: AR ← PC

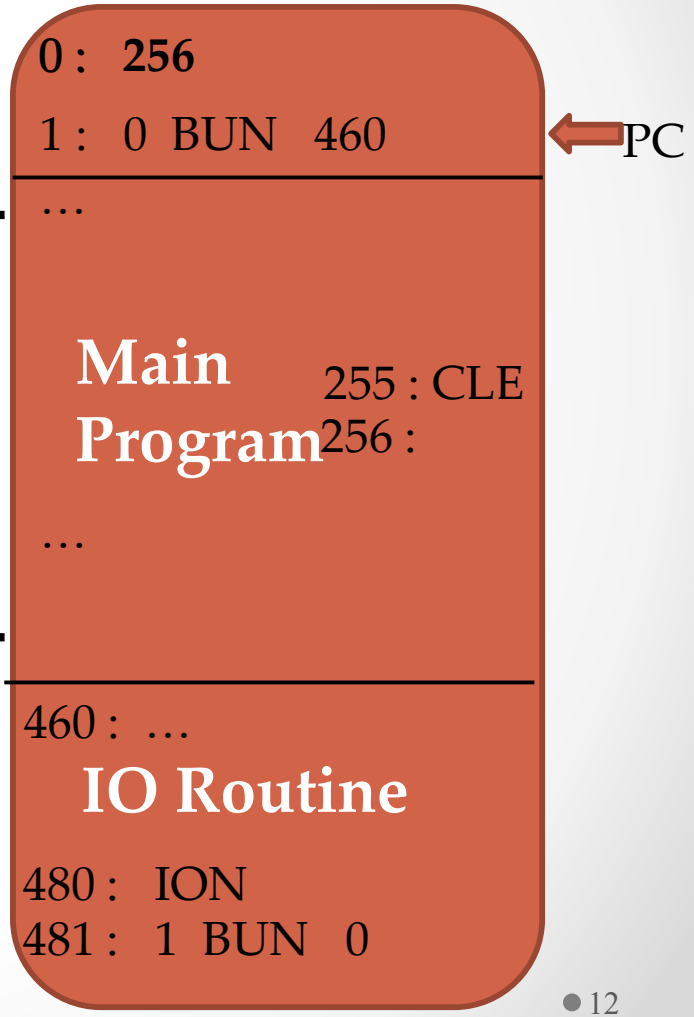
RT_0 : AR ← 0, TR ← PC

$R'T_1$: IR ← M[AR],
PC ← PC + 1

RT_1 : M[AR] ← TR ,
PC ← 0

$R'T_2$: D_0 ,.., D_7 ←
Decode IR(12-14)
AR ← IR(0-11),
I ← IR(15)

RT_2 : PC ← PC + 1,
IEN ← 0,
R ← 0, SC ← 0



IEN	I	IR	PC	AR	R	line
						1
						480
						481

Flowchart for computer operation

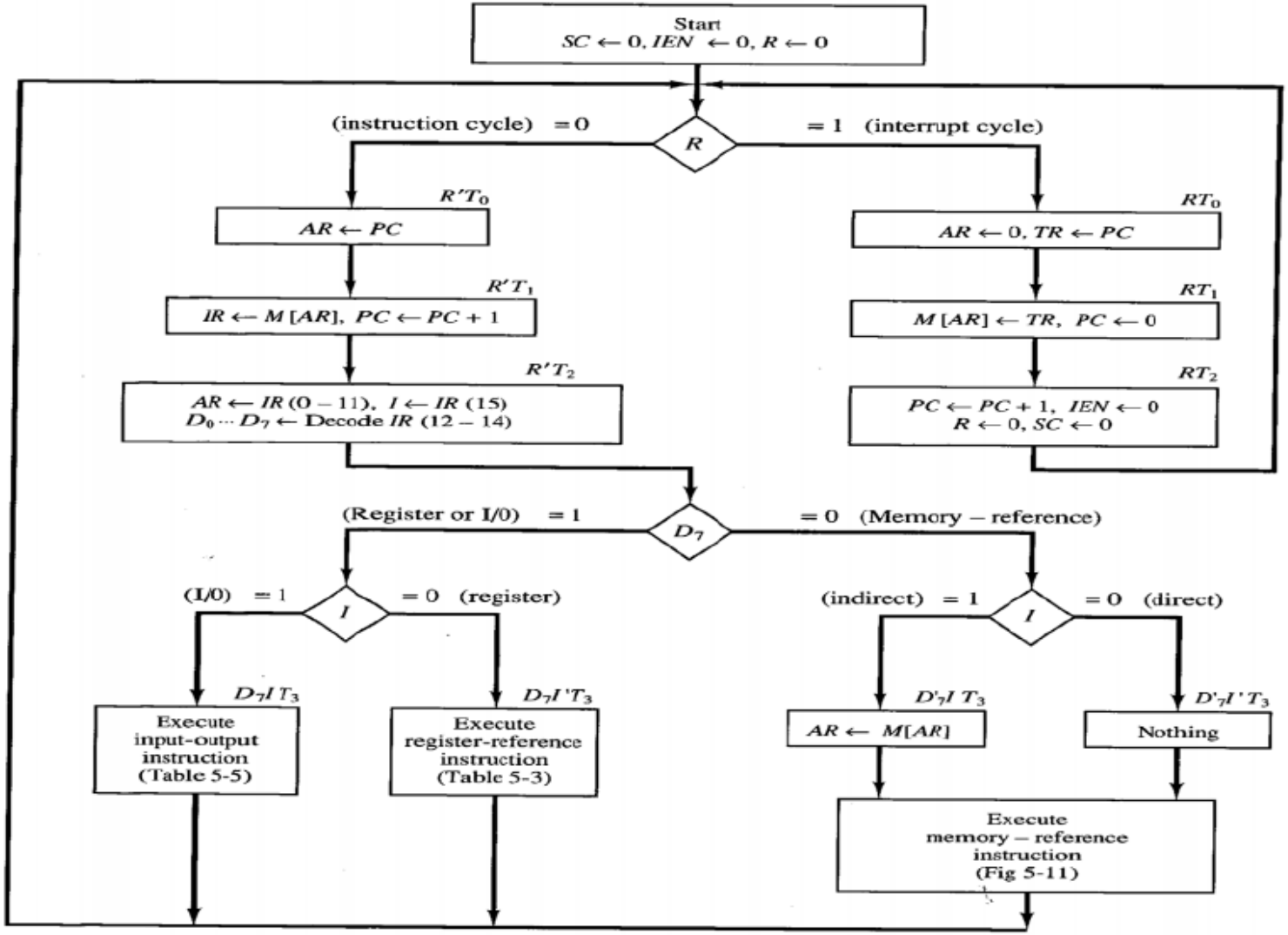


Figure 5-15 Flowchart for computer operation.

Summery of Control Functions & Microoperations

Fetch	$R'T_0$:	$AR \leftarrow PC$
	$R'T_1$:	$IR \leftarrow M[AR]$, $PC \leftarrow PC + 1$
Decode	$R'T_2$:	$D_0, \ldots, D_7 \leftarrow$ Decode $IR(12\text{–}14)$,
		$AR \leftarrow IR(0\text{–}11)$, $I \leftarrow IR(15)$
Indirect	$D_7'IT_3$:	$AR \leftarrow M[AR]$
Interrupt:		
$T_0'T_1'T_2'(IEN)(FGI + FGO)$:		$R \leftarrow 1$
	RT_0:	$AR \leftarrow 0$, $TR \leftarrow PC$
	RT_1:	$M[AR] \leftarrow TR$, $PC \leftarrow 0$
	RT_2:	$PC \leftarrow PC + 1$, $IEN \leftarrow 0$, $R \leftarrow 0$, $SC \leftarrow 0$
Memory-reference:		
AND	D_0T_4:	$DR \leftarrow M[AR]$
	D_0T_5:	$AC \leftarrow AC \wedge DR$, $SC \leftarrow 0$
ADD	D_1T_4:	$DR \leftarrow M[AR]$
	D_1T_5:	$AC \leftarrow AC + DR$, $E \leftarrow C_{out}$, $SC \leftarrow 0$
LDA	D_2T_4:	$DR \leftarrow M[AR]$
	D_2T_5:	$AC \leftarrow DR$, $SC \leftarrow 0$
STA	D_3T_4:	$M[AR] \leftarrow AC$, $SC \leftarrow 0$
BUN	D_4T_4:	$PC \leftarrow AR$, $SC \leftarrow 0$
BSA	D_5T_4:	$M[AR] \leftarrow PC$, $AR \leftarrow AR + 1$
	D_5T_5:	$PC \leftarrow AR$, $SC \leftarrow 0$
ISZ	D_6T_4:	$DR \leftarrow M[AR]$
	D_6T_5:	$DR \leftarrow DR + 1$
	D_6T_6:	$M[AR] \leftarrow DR$, if $(DR = 0)$ then $(PC \leftarrow PC + 1)$, $SC \leftarrow 0$

Summery of Control Functions & Microoperations

Register-reference:

$D_7 I' T_3 = r$ (common to all register-reference instructions)
$IR(i) = B_i$ $(i = 0, 1, 2, \ldots, 11)$

	r:	$SC \leftarrow 0$
CLA	rB_{11}:	$AC \leftarrow 0$
CLE	rB_{10}:	$E \leftarrow 0$
CMA	rB_9:	$AC \leftarrow \overline{AC}$
CME	rB_8:	$E \leftarrow \overline{E}$
CIR	rB_7:	$AC \leftarrow \text{shr } AC,\quad AC(15) \leftarrow E,\quad E \leftarrow AC(0)$
CIL	rB_6:	$AC \leftarrow \text{shl } AC,\quad AC(0) \leftarrow E,\quad E \leftarrow AC(15)$
INC	rB_5:	$AC \leftarrow AC + 1$
SPA	rB_4:	If $(AC(15) = 0)$ then $(PC \leftarrow PC + 1)$
SNA	rB_3:	If $(AC(15) = 1)$ then $(PC \leftarrow PC + 1)$
SZA	rB_2:	If $(AC = 0)$ then $PC \leftarrow PC + 1)$
SZE	rB_1:	If $(E = 0)$ then $(PC \leftarrow PC + 1)$
HLT	rB_0:	$S \leftarrow 0$

Input-output:

$D_7 I T_3 = p$ (common to all input–output instructions)
$IR(i) = B_i$ $(i = 6, 7, 8, 9, 10, 11)$

	p:	$SC \leftarrow 0$
INP	pB_{11}:	$AC(0\text{–}7) \leftarrow INPR,\quad FGI \leftarrow 0$
OUT	pB_{10}:	$OUTR \leftarrow AC(0\text{–}7),\quad FGO \leftarrow 0$
SKI	pB_9:	If $(FGI = 1)$ then $(PC \leftarrow PC + 1)$
SKO	pB_8:	If $(FGO = 1)$ then $(PC \leftarrow PC + 1)$
ION	pB_7:	$IEN \leftarrow 1$
IOF	pB_6:	$IEN \leftarrow 0$

QUIZ4

An output program resides in memory starting from address 2300.

It is executing after the computer recognizes an interrupt when FGO becomes a 1 (while IEN = 1).

1. What instruction must be placed at address 1?
2. What must be the last two instruction of the output program?

$R'T_0$: AR ← PC

RT_0 : AR ← 0, TR ← PC

$R'T_1$: IR ← M[AR],
PC ← PC + 1

RT_1 : M[AR] ← TR ,
PC ← 0

$R'T_2$: D_0 ,.., D_7 ←
Decode IR(12-14)
AR ← IR(0-11),
I ← IR(15)

RT_2 : PC ← PC + 1,
IEN ← 0,
R ← 0, SC ← 0

QUIZ4A

Implement the following instruction:

DEC : AC ← AC - 1

Register-reference:

$D_7 I' T_3 = r$ (common to all register-reference instructions)
$IR(i) = B_i$ $(i = 0, 1, 2, \ldots, 11)$

	r:	$SC \leftarrow 0$
CLA	rB_{11}:	$AC \leftarrow 0$
CLE	rB_{10}:	$E \leftarrow 0$
CMA	rB_9:	$AC \leftarrow \overline{AC}$
CME	rB_8:	$E \leftarrow \overline{E}$
CIR	rB_7:	$AC \leftarrow \text{shr } AC, \quad AC(15) \leftarrow E, \quad E \leftarrow AC(0)$
CIL	rB_6:	$AC \leftarrow \text{shl } AC, \quad AC(0) \leftarrow E, \quad E \leftarrow AC(15)$
INC	rB_5:	$AC \leftarrow AC + 1$
SPA	rB_4:	If $(AC(15) = 0)$ then $(PC \leftarrow PC + 1)$
SNA	rB_3:	If $(AC(15) = 1)$ then $(PC \leftarrow PC + 1)$
SZA	rB_2:	If $(AC = 0)$ then $PC \leftarrow PC + 1)$
SZE	rB_1:	If $(E = 0)$ then $(PC \leftarrow PC + 1)$
HLT	rB_0:	$S \leftarrow 0$